

AC822B Datasheet

Zhuhai Jieli Technology Co.,LTD

Version 1.3

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Revision History

Date	Revision	Author	Description
2023.08.10	V1.0	zh-jieli	Initial Release
2024.06.05	V1.1	zh-jieli	Modify IOVDD power supply range
2024.11.23	V1.2	zh-jieli	Add Peripherals Description
2025.04.07	V1.3	zh-jieli	Update Pin Description for APAN , APAP , PD0 , PD1

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AC822B Features

SYSTEM

- 32bit CPU 160MHz
- I-cache
- Support EMU
- On-chip SRAM 56kbyte
- Support MPU
- Built-In Flash
- 32KHz crystal oscillator
- Internal RC oscillator,PLL

Audio

- 1 x 16bit DAC
 - ❖ SNR 93dB
 - ❖ Noise 19uVrms
 - ❖ Sampling rate 8~96kHz
- 1 x 16bit Class-D Speaker Driver
 - ❖ SNR 96dB
 - ❖ Sampling rate 22.05~48kHz
 - ❖ Drive speaker directly 320mW @ 8Ω

Precise Measurement

- 1 x 24bit delta-sigma ADC
 - ❖ Single-ended or differential input
 - ❖ 6 channels external analog input
 - ❖ 5 channels internal analog input
 - ❖ PGA 1x/4x/8x/16x/32x/64x/128x
 - ❖ ENOB 21bits
 - ❖ Sampling rate 15Hz~7.7kHz
- 2 x OPA

Peripherals

- 1 x Full speed USB
- 4 x Multi-function 16bit timer
- 3 x UART interface
- 2 x I²C Master/Slave interface
- 2 x SPI Master/Slave interface
- 1 x 12bit 1Msps ADC(15 Channel)
- 43 x GPIO Support function remapping
- 12 x MCPWM
- 1 x Quadrature Rotate Decoder
- 1 x Parallel active port(8-bit)

- 1 x IR RX

LCD

- LDO driver up to 150 dot
- Bias 1/2,1/3,1/4
- 4x27 or 6x25 dots
- Concurrent IO function of LCD Interface

PMU

- Support deep sleep mode with RTC
- Support deep sleep mode with LCD
- Automatic wake-up of weighing scales
- VPWR range 2.7V to 5.5V
- IOVDD range 2.1V to 3.6V
- Charge pump for AVDDLCD
- Charge pump for AVDDCP

Packages

- LQFP64(7mm*7mm)

Temperature

- Operating temperature
 - TC = -20°C to +85°C(standard range)
 - TC = -40°C to +105°C(extended range)
- Storage temperature -65°C to +150°C

Applications

- 4-electrode body fat scale
- Sphygmomanometer
- Oximeter
- Ear thermometer

1 Block Diagram

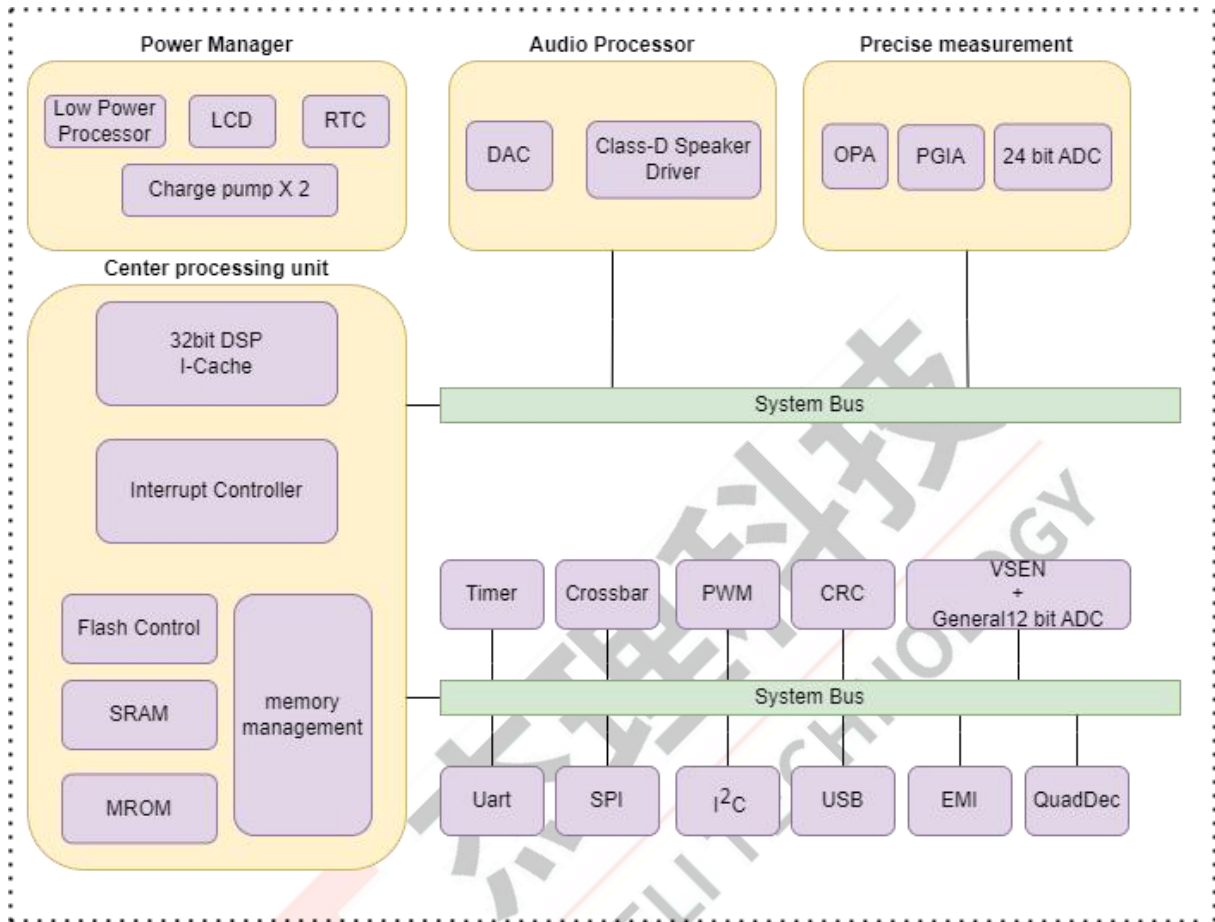


Figure 1-1 AC822B Block Diagram

2 Pin Definition

2.1 Pin Assignment

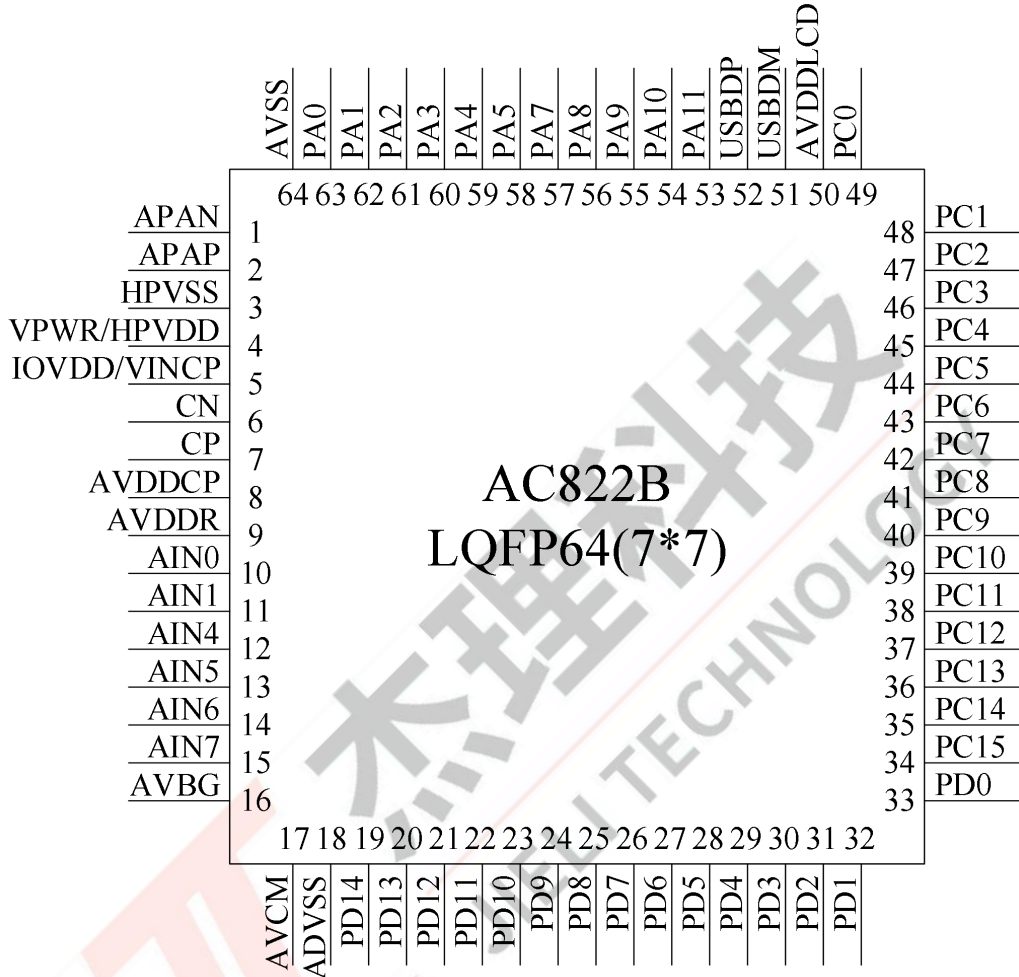


Figure 2-1 AC822B Pin Assignment

2.2 Pin Description

Table 2-2-1 AC822B Pin Description

Pin No.	Name	Type	IO Initial State	Description
1	APAN	O	--	Class-D Speaker Driver Negative Output
2	APAP	O	--	Class-D Speaker Driver Positive Output
3	HPVSS	G	--	Class-D Speaker Driver Ground
4	VPWR	P	--	Power Input
	HPVDD	P	--	Class-D Speaker Driver Power
5	IOVDD	P	--	IO Power
	VINCP	P	--	--
6	CN	P	--	--
7	CP	P	--	--
8	AVDDCP	P	--	--
9	AVDDR	P	--	--
10	AIN0	I	--	PGIA Analog Input Channel0
11	AIN1	I	--	PGIA Analog Input Channel1
12	AIN4	I	--	PGIA Analog Input Channel4
13	AIN5	I	--	PGIA Analog Input Channel5
14	AIN6	I	--	PGIA Analog Input Channel6
15	AIN7	I	--	PGIA Analog Input Channel7
16	AVBG	P	--	Audio and 24bit delta-sigma ADC Reference Voltage
17	AVCM	P	--	24bit delta-sigma ADC Common-Mode Voltage
18	ADVSS	G	--	24bit delta-sigma ADC Ground
19	PD14	I/O	Z	LCD SEG26
20	PD13	I/O	Z	LCD SEG25
21	PD12	I/O	Z	LCD SEG24
22	PD11	I/O	Z	LCD SEG23
				TIMER3 PWM
23	PD10	I/O	Z	LCD SEG22
				TIMER2 PWM
24	PD9	I/O	Z	LCD SEG21
				TIMER1 PWM
25	PD8	I/O	Z	LCD SEG20
				TIMER0 PWM
26	PD7	I/O	Z	LCD SEG19
				MCPWM5 L
27	PD6	I/O	Z	LCD SEG18
				MCPWM5 H
28	PD5	I/O	Z	LCD SEG17
				MCPWM4 L

Pin No.	Name	Type	IO Initial State	Description
29	PD4	I/O	Z	LCD SEG16 MCPWM4 H
30	PD3	I/O	Z	LCD SEG15 MCPWM3 L
31	PD2	I/O	Z	LCD SEG14 MCPWM3 H
32	PD1	I/O	Z	LCD SEG13 PAP RDE
33	PD0	I/O	Z	LCD SEG12 PAP WRE
34	PC15	I/O	Z	LCD SEG11 PAP DAT7
35	PC14	I/O	Z	LCD SEG10 PAP DAT6
36	PC13	I/O	Z	LCD SEG09 PAP DAT5
37	PC12	I/O	Z	LCD SEG08 PAP DAT4
38	PC11	I/O	Z	LCD SEG07 PAP DAT3 MCPWM0_FPI
39	PC10	I/O	Z	LCD SEG06 PAP DAT2
40	PC9	I/O	Z	LCD SEG05 PAP DAT1
41	PC8	I/O	Z	LCD SEG04 PAP DAT0
42	PC7	I/O	Z	LCD SEG03
43	PC6	I/O	Z	LCD SEG02
44	PC5	I/O	Z	LCD SEG01 LCD COM5
45	PC4	I/O	Z	LCD SEG00 LCD COM4
46	PC3	I/O	Z	LCD COM3
47	PC2	I/O	Z	LCD COM2
48	PC1	I/O	Z	LCD COM1
49	PC0	I/O	Z	LCD COM0
50	AVDDLCD	P	--	LCD power output
51	USBDM	I/O	15kΩ Pull-down	ADC14(ADC Input Channel 14)
52	USBDP	I/O	15kΩ Pull-down	ADC13(ADC Input Channel 13)

Pin No.	Name	Type	IO Initial State	Description
53	PA11	I/O	Z	ADC11(ADC Input Channel 11) LVD(External Low Voltage Detection Input)
54	PA10	I/O	Z	ADC10(ADC Input Channel 10)
55	PA9	I/O	Z	ADC9(ADC Input Channel 9)
56	PA8	I/O	Z	ADC8(ADC Input Channel 8) 32k Crystal Oscillator Output MCPWM0_CK1
57	PA7	I/O	Z	ADC7(ADC Input Channel 7) 32k Crystal Oscillator Input
58	PA5	I/O	Z	ADC5(ADC Input Channel 5) VSEN3(VSENSOR Input Channel 3)
59	PA4	I/O	Z	ADC4(ADC Input Channel 4) VSEN2(VSENSOR Input Channel 2)
60	PA3	I/O	Z	ADC3(ADC Input Channel 3) VSEN1(VSENSOR Input Channel 1)
61	PA2	I/O	Z	ADC2(ADC Input Channel 2) VSEN0(VSENSOR Input Channel 0)
62	PA1	I/O	Z	ADC1(ADC Input Channel 1)
63	PA0	I/O	10kΩ Pull-up	ADC0(ADC Input Channel 0) Hold down 0 to reset
64	AVSS	G	--	Audio Ground

Note

- 1.IO initial state abbreviations Z--High resistance, H--High level, L--Low level, X--May be changed during power on.
2. MCPWM0/1/2, UART, I²C, I²S, SPI1/2, IR RX functions can be remapped to any I/O.
- 3.PAP_WRE, PAP_RDE, TIMER functions also can be remapped to any I/O.

Table 2-2-2 Pin Types Description

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
G	Ground	I	Input
RF	RF antenna	O	Output

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-20	+85	°C
Tstg	Storage temperature	-65	+150	°C
VPWR	Supply Voltage	-0.3	6	V
IOVDD		-0.3	3.6	V
AVDDLCD		-0.3	5	V
AVDDCP		-0.3	6	V
AVDDR		-0.3	3.6	V
HPVDD		-0.3	6	V
AVBG		Audio Reference Voltage	-0.3	3.6
AVCM	Common-Mode Voltage	-0.3	3.6	V
GPIO	Input voltage of GPIO (except PC0~PC15/PD0~PD14)	-0.3	3.6	V
HVTIO	Input voltage of HVT-IO (PC0~PC15/PD0~PD14)	-0.3	6	V

Note

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

3.2 ESD Ratings

Table 3-2 ESD Ratings

Parameter	Typ	Test pin	Reference standard
Human Body Mode	±4kV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2kV	All pins	JEDEC EIA/JESD22-C101F

3.3 PMU Characteristics

Table 3-3-1 PMU Characteristics under VPWR supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPWR	Power supply	--	2.7	--	5.5	V
HPVDD	Power supply	--	2.7	--	5.5	V
Operating mode						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Voltage output	--	--	3	--	V
	Loading current	IOVDD=3.0V@VPWR = 3.7V	--	--	120	mA
Low Power mode						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Loading current	IOVDD=3.0V@VPWR = 3.7V	--	--	10	mA

Table 3-3-2 PMU Characteristics under IOVDD supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IOVDD	Power supply	--	2.1	--	3.6	V

Table 3-3-3 PMU Sub-module Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AVDDLCD	Voltage output	--	--	4.2	--	V
	Loading current	AVDDLCD=4.2V@IOVDD = 3.0V	--	--	350	uA
AVDDCP	Voltage output	--	--	3.6	--	V
	Loading current	AVDDCP=3.6V@IOVDD = 3.0V	--	--	40	mA
AVDDR	Voltage output	--	--	3.0	--	V
	Loading current	AVDDCP=3.6V@IOVDD = 3.0V	--	--	20	mA

Note

1.Power on sequence rule: VPWR and HPVDD are powered on simultaneously, or VPWR is powered on earlier than HPVDD.

3.4 IO Characteristics

Table 3-4 IO Characteristics

Input Characteristics						
Symbol	Parameter	Conditions	IO	Min	Max	Unit
V _{IL}	Low-Level Input Voltage	IOVDD = 3.0V	PA0~PA5 PA7~PA11 PC0~PC15 PD0~PD14 USBDP USBDM	-0.3	1.4	V
			PA0~PA5 PA7~PA11 USBDP USBDM			
V _{IH}	High-Level Input Voltage	IOVDD = 3.0V	PA0~PA5 PA7~PA11 USBDP USBDM	1.7	3.3	V
		IOVDD = 3.0V	PC0~PC15 PD0~PD14	1.7	5.5	V
Output Characteristics						
Symbol	Parameter	Conditions	IO	Typ	Unit	
I _{OL}	Output Current	IOVDD = 3.0V Voutput = 0.3V	PA0~PA5 PA7~PA11	2(HD=0) 6(HD=1) 20(HD=2) 45(HD=3)	mA	
		IOVDD = 3.0V Voutput = 0.3V	PC0~PC15 PD0~PD14	8	mA	

			USBDP USBDM			
I _{OH}	Output Current	IOVDD = 3.0V Voutput = 2.7V	PA0~PA5 PA7~PA11	2(HD=0) 6(HD=1) 20(HD=2) 45(HD=3)	mA	
		IOVDD = 3.0V Voutput = 2.7V	PC0~PC15 PD0~PD14 USBDP USBDM	8	mA	
Internal Resistance Characteristics						
Symbol	Parameter	Conditions	IO	Typ	Unit	
R _{pu}	Pull-up Resistance	IOVDD = 3.0V	PA0~PA5 PA7~PA11 PC0~PC15 PD0~PD14	10k(PU=1) 100k(PU=2) 1M(PU=3)	Ω	
			IOVDD = 3.0V	USBDP	1.5k	Ω
			IOVDD = 3.0V	USBDM	180k	Ω
Symbol	Parameter	Conditions	IO	Typ	Unit	
R _{pd}	Pull-down Resistance	IOVDD = 3.0V	PA0~PA5 PA7~PA11 PC0~PC15 PD0~PD14	10k(PD=1) 100k(PD=2) 1M(PD=3)	Ω	
			IOVDD = 3.0V	USBDP USBDM	15k	Ω

Note

1. Internal pull-up/pull-down resistance accuracy ±20%.

3.5 Audio DAC Characteristics

Table 3-5 Audio DAC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	--	16	bits
Sample Rate	--	8	--	96	kHz
SNR	Single-ended Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=100kΩ	--	93	--	dB
Dynamic Range	Single-ended Mode Fin=1kHz@-60dBFS Fs=44.1kHz	--	93	--	dB

Parameter	Conditions	Min	Typ	Max	Unit
	B/W=20Hz~20kHz A-Weighted Load=100kΩ				
THD+N	Single-ended Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=100kΩ	--	-76	--	dB
Noise Floor	Single-ended Mode B/W=20Hz~20kHz A-Weighted Load=100kΩ	--	19	--	uVrms
Max Amplitude	Single-ended Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=100kΩ THD+N<0.1%	--	0.8	--	Vrms

3.6 Class-D Speaker Driver Characteristics

Table 3-6 Class-D Speaker Driver Characteristics under HPVDD 3.7V

Parameter	Conditions	Min	Typ	Max	Unit
Resolution	--	--	--	16	bits
Input Sample Rate	--	22.05	--	48	kHz
SNR	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	96	--	dB
	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=8Ω	--	96	--	dB
THD+N	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	-75	--	dB
	Differential Mode Fin=1kHz@0dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted	--	-45	--	dB

Parameter	Conditions	Min	Typ	Max	Unit
	Load=8Ω				
Noise Floor	Differential Mode B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	30	--	uVrms
	Differential Mode B/W=20Hz~20kHz A-Weighted Load=8Ω	--	32	--	uVrms
Dynamic Range	Differential Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=10kΩ	--	89	--	dB
	Differential Mode Fin=1kHz@-60dBFS Fs=44.1kHz B/W=20Hz~20kHz A-Weighted Load=8Ω	--	89	--	dB

3.7 12bit ADC Characteristics

Table 3-7-1 12bit ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
AVDD(ADC Supply Voltage)	AVDD=IOVDD	2.1	3	3.6	V
AVREF(ADC Positive reference voltage)	--	2.1	3	AVDD	V
AVSSREF(ADC Negative reference voltage)	--	--	0	--	V
I _{AVDD} (Current of the ADC on AVDD and AVREF)	Single-ended f _{ADC} =12MHz AVDD=AVREF=3V	--	310	--	uA
	Diff-ended with DiffAMP f _{ADC} =12MHz AVDD=AVREF=3V	--	780	--	uA
f _{ADC} (ADC Clock Frequency)	--	0.25	--	12	MHz
T _s (ADC Sampling Time)	--	1.5	--	--	1/f _{ADC}
ADC Conversion Time	Including Sampling Time	8	14	14	1/f _{ADC}
ADC Input Voltage Range	--	0	--	AVREF	V
ADC Internal Sample and Hold Capacitor	--	--	--	5	pF
Sampling Switch Resistance	--	--	--	1	kΩ
External Input Impedance	T _s =1.5/f _{ADC}	--	--	1.5	kΩ
	T _s >=50/f _{ADC}	--	--	50	kΩ
ADC Resolution	Programmable	6	12	12	bit

Parameter	Conditions	Min	Typ	Max	Unit
INL	AVDD=3V, f _{ADC} =12MHz	-1	--	3	LSB
DNL	AVDD=3V, f _{ADC} =12MHz	-1	--	1	LSB
ADC Offset Error	AVDD=3V, f _{ADC} =12MHz	--	--	2.4	LSB
Gain Error	AVDD=3V, f _{ADC} =12MHz	--	--	5.8	LSB
ENOB(Effective number of bits)	Single-ended AVDD=AVREF=3V f _{IN} =1kHz, f _{ADC} =12MHz	--	10.6	--	bit
	Diff-ended with DiffAMP AVDD=AVREF=3V f _{IN} =1kHz, f _{ADC} =12MHz	--	11	--	bit

Table 3-7-2 12bit ADC Characteristics

T _{sample} (1/f _{ADC})	T _{sample} (us)	Max.Rext-input(kΩ)
1.5	0.125	1.5
7.5	0.625	10
13.5	1.125	15
25.5	2.125	25
49.5	4.125	50
97.5	8.125	--

3.8 24bit delta-sigma ADC Characteristics

Table 3-8-1 24bit delta-sigma ADC Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
I _{ADC} (Current of the ADC on AVDDR)	AVDD=IOVDD	--	1.4	--	mA
F _{SMP} (Data rate)	--	15	--	7692	Hz
V _{AIN_MAX} (Full-scale input voltage)	Differential(V _{ip} -V _{in})	--	--	1.4	V
V _{AIN} (PGIA input absolute voltage)	PGA_INP and PGA_INN absolute input voltage	0.2	--	AVDDR-1	V
V _x (PGIA output absolute voltage)	PGIA absolute output voltage	0.2	--	AVDDR-0.2	V
Noise Free Bits	Gain = 1,V _{ref} = 2.0V,F _{SMP} = 15Hz, Positive and Negative input internally Connect to AVCM	--	18.7	--	bit
	Gain = 128,V _{ref} = 2.0V,F _{SMP} =15Hz, Positive and Negative input internally Connect to AVCM	--	14.6	--	bit
ENOB	Gain = 1,V _{ref} = 2.0V,F _{SMP} = 15Hz, Positive and Negative input internally Connect to AVCM	--	21	--	bit
	Gain = 128, V _{ref} = 2.0V,F _{SMP} = 15Hz, Positive and Negative input internally Connect to AVCM	--	17	--	bit

Table 3-8-2 24bit delta-sigma ADC Characteristics

24bit delta-sigma ADC Performance Noise Free Bit vs. Output Rate and Gain								
Output Sample Rate(Hz)	15.3	30.6	61.2	122	489	1976	3875	7692
PGIA GAIN 1x1	18.8	18.4	18.0	17.5	16.3	15.1	13.9	12.3
PGIA GAIN 4x1	18.5	18.1	17.7	17.2	15.9	14.9	13.9	12.3
PGIA GAIN 8x1	18.0	17.8	17.4	16.9	15.7	14.7	13.8	11.6
PGIA GAIN 16x1	17.3	17.1	16.8	16.4	15.2	13.9	13.3	11.8
PGIA GAIN 32x1	16.4	16.4	16.0	15.7	14.4	13.4	12.5	10.9
PGIA GAIN 64x1	15.5	15.3	15.2	14.6	13.5	12.4	11.8	10.6
PGIA GAIN 128x1	14.7	14.5	14.1	13.8	12.5	11.4	10.8	9.8

4 Package Information

4.1 LQFP64_7×7mm

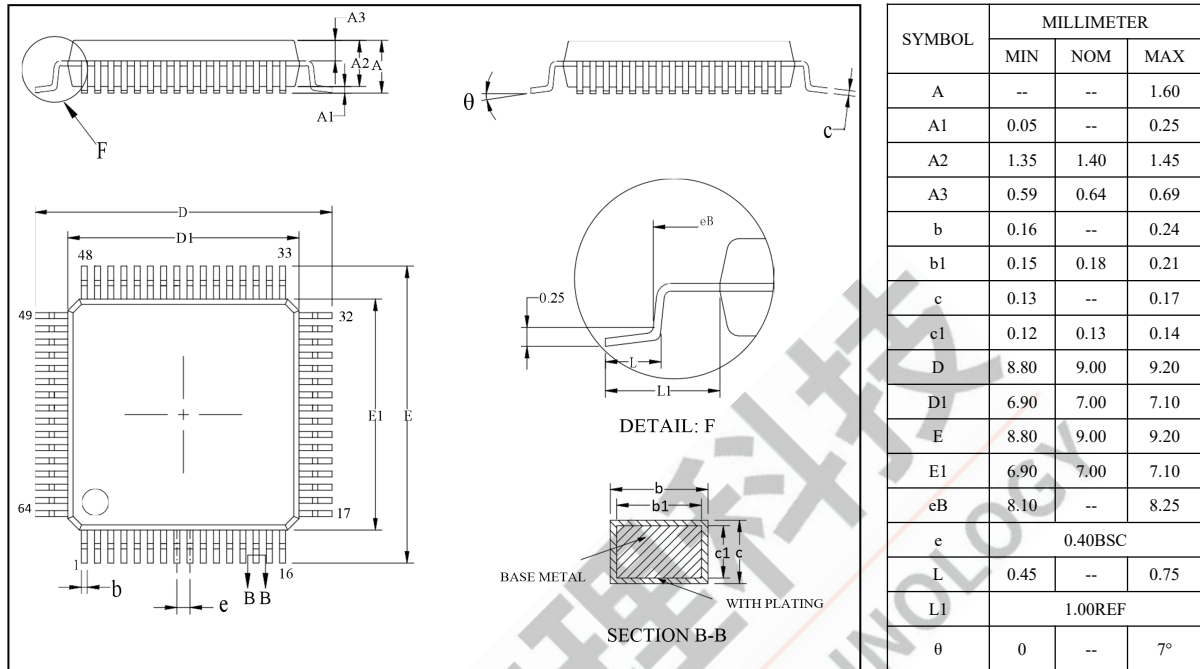


Figure 4-1 AC822B Package

5 IC Marking Information

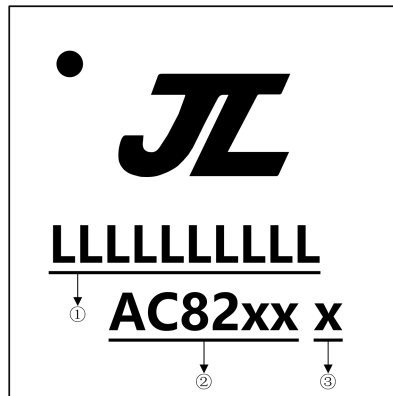


Figure 5-1 AC822B Package Outline

- ① Production Batch
- ② Chip Model
- ③ Built-in flash size
 - 4 4Mbit Flash
 - 8 8Mbit Flash

6 Solder-Reflow Condition

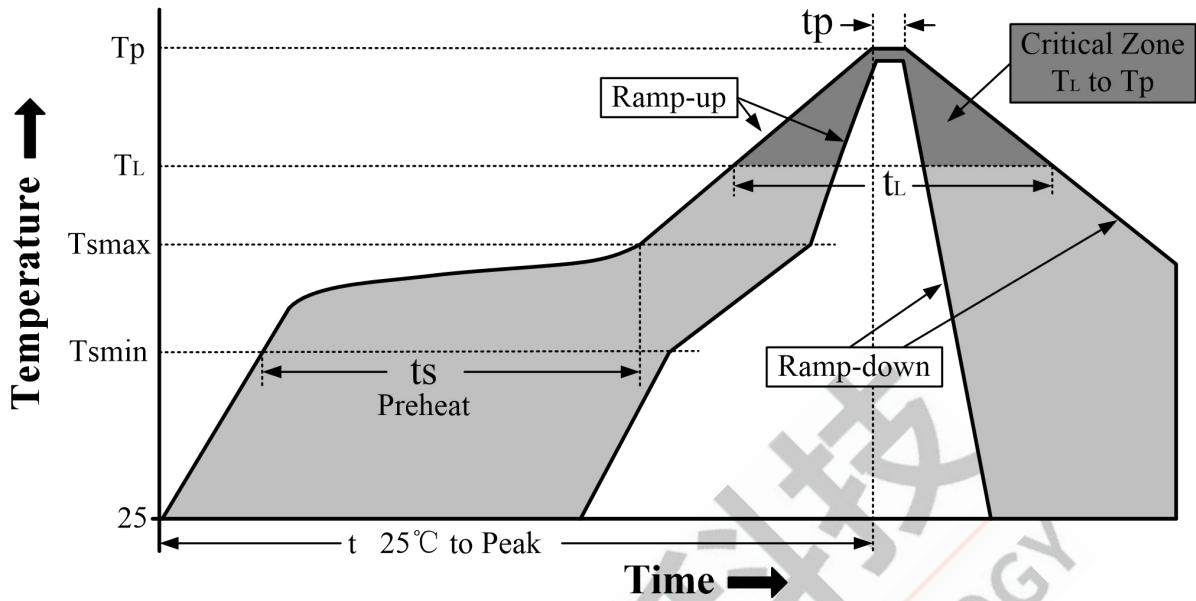


Figure 6-1 Classification Reflow Profile

Table 6-1 Classification Profiles

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak	Temperature Min (T_{smin})	100°C	150°C
	Temperature Max (T_{smax})	150°C	200°C
	Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3°C/second max	3°C/second max
Liquidus temperature (T_L)		183°C	217°C
Time (t_L) maintained above T_L		60-150 seconds	60-150 seconds
Peak package body temperature (T_p)		See Table 6-2	See Table 6-3
Time within 5°C of actual Peak Temperature (t_p) ²		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6°C/second max	6°C/second max
Time 25°C to peak temperature		6 minutes max	8 minutes max

Note

1. All temperatures refer to topside of the package, measured on the package body surface
2. Time within 5°C of actual peak temperature (t_p) specified for the reflow profiles is a "supplier" and "user" maximum.

Table 6-2 SnPb Classification Temperature

Package Thickness	Volume mm ³	Volume mm ³
	< 350	≥ 350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

Table 6-3 Pb-free - Classification Temperature

Package Thickness	Volume mm ³ < 350	Volume mm ³ 350 - 2000	Volume mm ³ > 2000
< 1.6mm	260°C	260°C	260°C
1.6 mm - 2.5mm	260°C	250°C	245°C
> 2.5mm	250°C	245°C	245°C

Note

1.*Tolerance The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C.For example 260°C+0°C)at the rated MSL level.