AC983A Datasheet

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AC983A Features

CPU

- 8051 CPU

Memory

- On-chip RAM
- On-chip OTP
- Optional built-in flash memory

Clocks

- On-chip 200 KHz low-power-consumption clock oscillator
- On-chip 32 MHz lower-temperature-drift clock oscillator

Peripherals

- One low voltage detector
- 5-channel 10-bit general purpose ADC
- One multi-function 8-bit timer0, support capture and PWM mode
- One multi-function 16-bit timer1, support capture and PWM mode
- Three PWM generator for LED driving
- Two UART interface
- One Lightning charging host
- One Qi Wireless Charge protocol controller
- Support Off-Chip NTC Resistance
- 10 Individually programmable and multiplexed GPIO pins
- Up to 4 external interrupt / wake-up source

PMU

- 5uA standby current
- 8uA Timed wake-up current
- 3mA Operating current
- 15V input withstand voltage
- Linear charger, programmable chargecurrent Up to 400mA
- Support 4.2V and 4.35V lithium batteries
- Trickle / constant current / constant voltage three-stage charging
- Cut-off charge current：C/10
- Synchronous boost output 5V/200mA, efficiency up to 91%@0.1A
- Support Earphone communication
- Overcurrent, Short circuit and overvoltage protection of discharge module
- VPWR range : 4.5V to 5.5V
- VBAT range : 3.0V to 4.5V
- IOVDD range : 2.7V to 3.4V

Packages

- SOP16

Temperature

- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

Applications

- Bluetooth TWS charging Box

1 Block Diagram

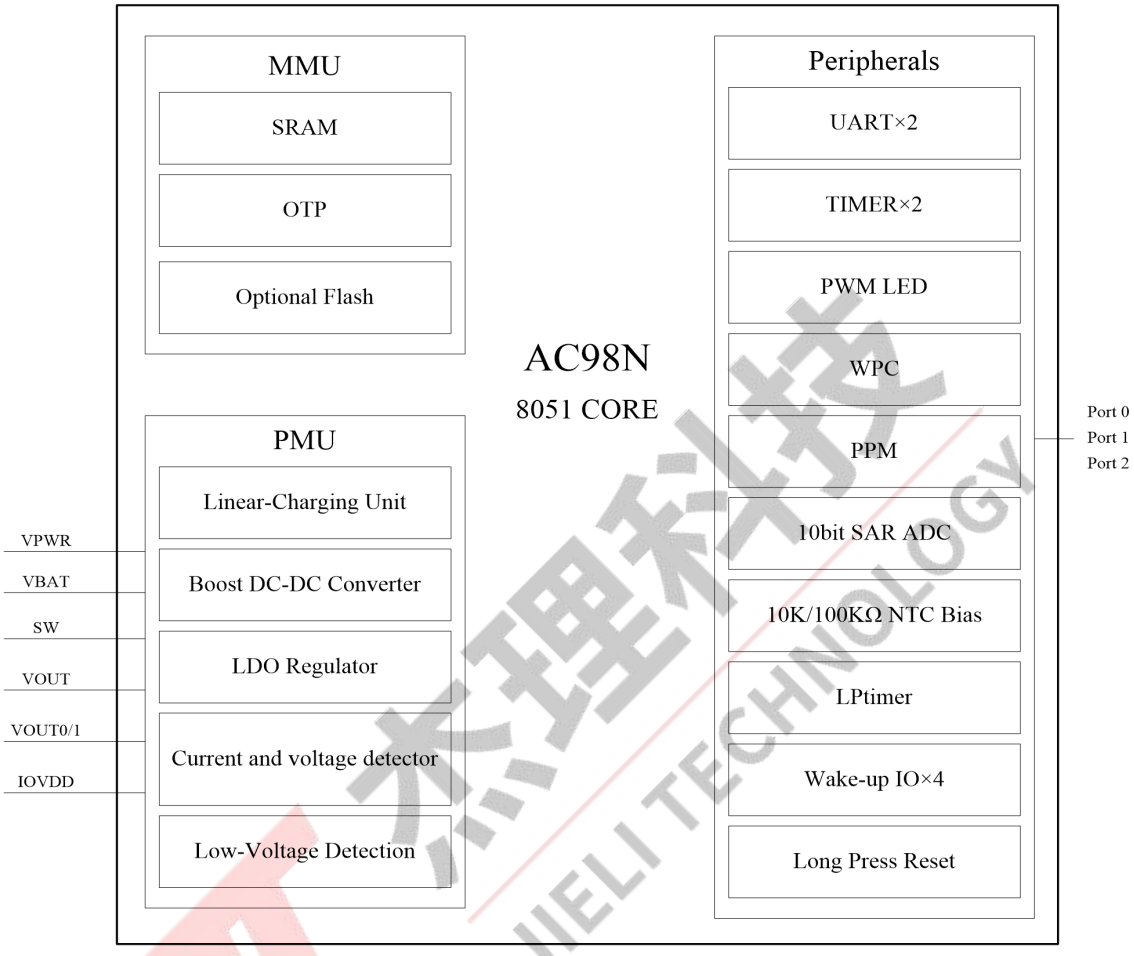


Figure 1-1 AC983A Block Diagram

2 Pin Definition

2.1 Pin Assignment

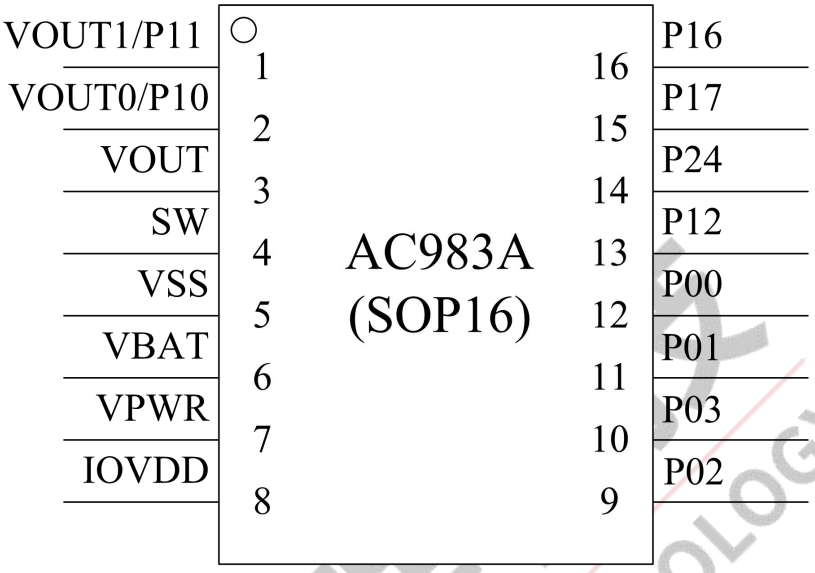


Figure 2-1 AC983A Package Diagram

2.2 Pin Description

Table 2-1 AC983A Pin Description

PIN NO.	Name	Type	Function	Other Function
1	VOUT1	PO		VOUT1:Boost Output Path 1;
	P11	I/O	GPIO (High Voltage Resistant)	UART1TXA:Uart1 Data Output(A); UART1RXA:Uart1 Data Input(A);
2	VOUT0	PO		VOUT0:Boost Output Path 0;
	P10	I/O	GPIO (High Voltage Resistant)	UART0TXA:Uart0 Data Output(A); UART0RXA:Uart0 Data Input(A);
3	VOUT	PO		Boost Power Output;
4	SW	O		Switch signal of the Buck converter,Connected to inductor;
5	VSS	G		System ground;
6	VBAT	P		Battery interface;
7	VPWR	PI		Charge Power Input;
8	IOVDD	PO	Power supply for GPIO	Built-in linear voltage regulator output;
9	P02	I/O	GPIO	LED2_A:LED2 Controller Output(A); ADC2:ADC Input Channel 2;
10	P03	I/O	GPIO	TMR0_PWM :Timer0 PWM Output; TMR0_CIN: Timer0 Clock In; ADC3:ADC Input Channel 3;
11	P01	I/O	GPIO	LED1_A:LED1 Controller Output(A); UART0TXB:Uart0 Data Output(B); TMR1_PWM :Timer1 PWM Output; TMR1_CIN: Timer1 Clock In; ADC1:ADC Input Channel 1;
12	P00	I/O	GPIO (pull down)	LED0_A:LED0 Controller Output(A); UART0RXB:Uart0 Data Input(B); ADC0:ADC Input Channel 0;
13	P12	I/O	GPIO	VPP:OTP program voltage input;
14	P24	I/O	GPIO (High Voltage Resistant)	PPM_DAT(A):Power protocol master control(A);
15	P17	I/O	GPIO	WPR_TX1:Wireless Power Receiver Data1; Updata:Support built-in flash memory Updata;
16	P16	I/O	GPIO	NTC:Built-in 10KΩ or 100KΩ bias resistors; LVD:Low Voltage Detection; ADC7:ADC Input Channel 7;

Pin Type	Description	Pin Type	Description
P	Power	I/O	Input or Output
PI	Power Input	PO	Power Output
G	Ground	O	Output

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1

Symbol	Parameter	Min	Max	Unit
Topt	Operating temperature	-40	+85	℃
Tstg	Storage temperature	-65	+150	℃
VBAT	Supply Voltage	-0.3	5.5	V
VPWR	Charger Voltage	-0.3	15	V
V_{IOVDD}	Voltage applied at IOVDD	-0.3	3.6	V
V_{GPIO}	Voltage applied to GPIO	-0.3	IOVDD+0.3	V
V_{HVIO}	Voltage applied to High Voltage Resistant IO	-0.3	+5.5	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below.

3.2 ESD Protectio

Table 3-2

Parameter	Typ.	Test pin	Reference standard
Human Body Mode	±4KV	All pins	JEDEC EIA/JESD22-A114
Machine Mode	±200V	All pins	JEDEC EIA/JESD22-A115
Charge Device Model	±2KV	All pins	JEDEC EIA/JESD22-C101F
Latch up	±200mA	All GPIO pins	JEDEC STANDARD NO.78E
	1.5xVopmax	All power pins	

Note : 1.5xVopmax = 1.5 times maximum operating voltage.

3.3 PMU Characteristics

Table 3-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	3.0	3.7	4.5	V	_
VPWR	Charger supply Voltage	4.5	5.0	5.5	V	_
IOVDD	Voltage output	2.7	3.0	3.4	V	VBAT = 4.2V, 10mA loading
	Loading current	_	_	100	mA	IOVDD=3.3V@VBAT = 3.6V
V_{LVD}	Voltage input	2.4	2.8	3.0	V	Low-Voltage Detection of IOVDD

3.4 Battery Charge

Linear Charger **Table 3-4**

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{PWR}	Charge Input Voltage Range	4.5	5	5.5	V	VBAT=3.7V
$VPWR_{OV}$	VPWR Overvoltage	_	_	15	V	
$VPWR_{W-up}$	VPWR Wake-up voltage	2.0	_	_	V	VBAT=3.7V
$VPWR_{UV}$	Charging Undervoltage	_	3.0	_	V	
$V_{BAT\ Float}$	Battery Charge Termination Voltage	4.15	4.2	4.25	V	VPWR=5.0V
		4.30	4.35	4.40	V	
I_{CC}	Fast Charge Current	50	_	400	mA	VBAT=3.7V@VPWR=5.0V
I_{END}	Charge Termination Current Threshold	5	_	40	mA	
V_{Trikl}	Trickle Charge Voltage	_	3.0	_	V	VPWR=5.0V
I_{Trikl}	Trickle Charge Current	5	_	40	mA	$V_{BAT}<V_{Trikl}$
V_{RCH}	Recharging Voltage	4.0	4.1	4.15	V	

3.5 Boost Discharge

TA=25℃,L=2.2uH **Table 3-5**

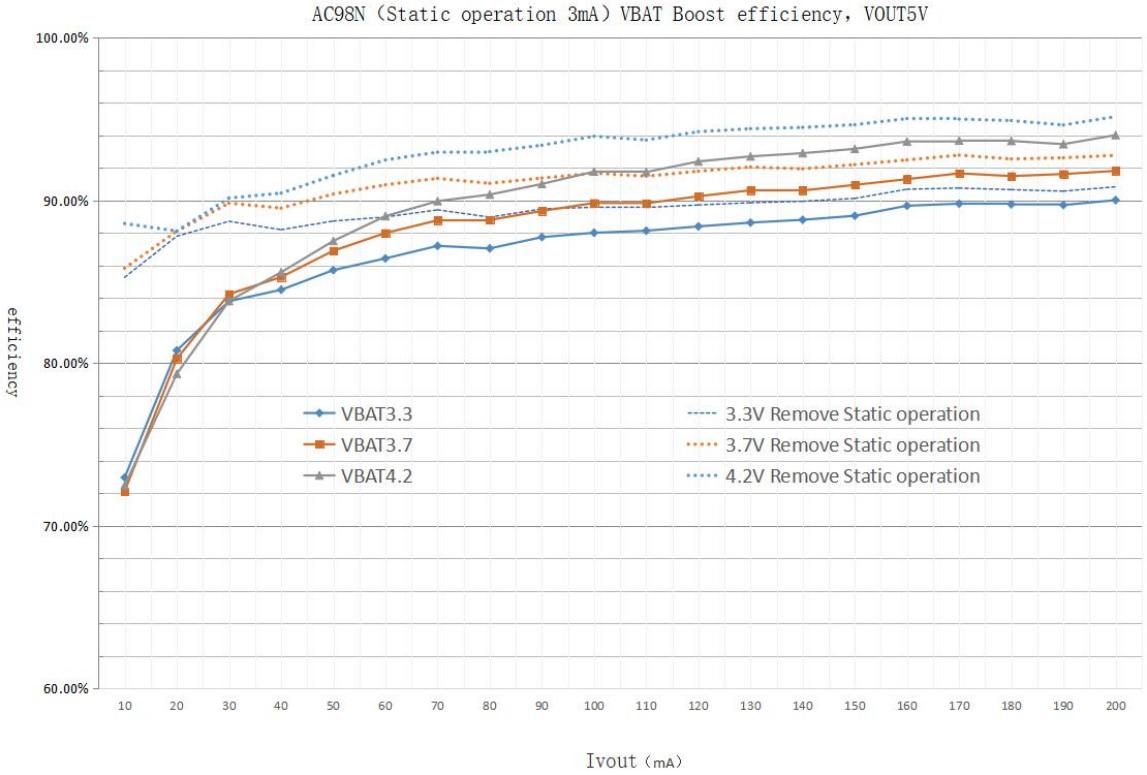
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Supply Voltage	3	3.7	4.5	V	
VOUT	Output Voltage Range	_	5	_	V	200mA@VBAT=3.7V
I_{VOUT}	Output Current	_	_	200	mA	VBAT=3.7V@VOUT=5V
η	Conversion efficiency	_	91	_	%	VBAT=3.7V@VOUT5V/100mA
V_{UV_BAT}	Battery undervoltage latching threshold voltage	3.0	3.3	_	V	I_{VOUT}=200mA
F_{SW}	Switching Frequency	_	_	1.0	MHz	
VO_{OVP}	Output overvoltage protection	_	5.5	_	V	

VO_{UV}	Output undervoltage protection	_	3.3	_	V	
$I_{Max-VOUT0/1}$	Overcurrent shutdown current	_	100	_	mA	
$R_{VOUT0/1}$	VOUT0/1 impedance	_	1.2	_	Ω	

3.6 Boost efficiency curve

(VOUT=5V, CIN=1μF, COUT=10μF, L=2.2μH, TA=25°C, unless otherwise noted.)

Table 3-6



3.7 IO Input/Output Electrical Logical Characteristics

Table 3-7

GPIO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD = 3.0V
High Voltage Resistant IO input characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.0V
V_{IH}	High-Level Input Voltage	0.7* IOVDD	–	+5V	V	IOVDD = 3.0V
GPIO & High Voltage Resistant IO output characteristics						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
V_{OL}	Low-Level Output Voltage	–	–	0.1* IOVDD	V	IOVDD = 3.0V
V_{OH}	High-Level Output Voltage	0.9* IOVDD	–	–	V	IOVDD = 3.0V

Resistant IO output characteristics					
Symbol	**Parameter**	**GPIO**	**Typ**	**Unit**	**Test Conditions**
V_{OL}	0.1*IOVDD Drive current	P00~P03 P16~P17	HD=0 : -3.5 HD=1 : -33	mA	IOVDD = 3.0V
		P10~P12 P24	-10		
V_{OH}	0.9*IOVDD Drive current	P00~P03 P16~P17	HD=0 : 3.5 HD=1 : 10	mA	IOVDD = 3.0V
		P10~P12 P24	8.5		

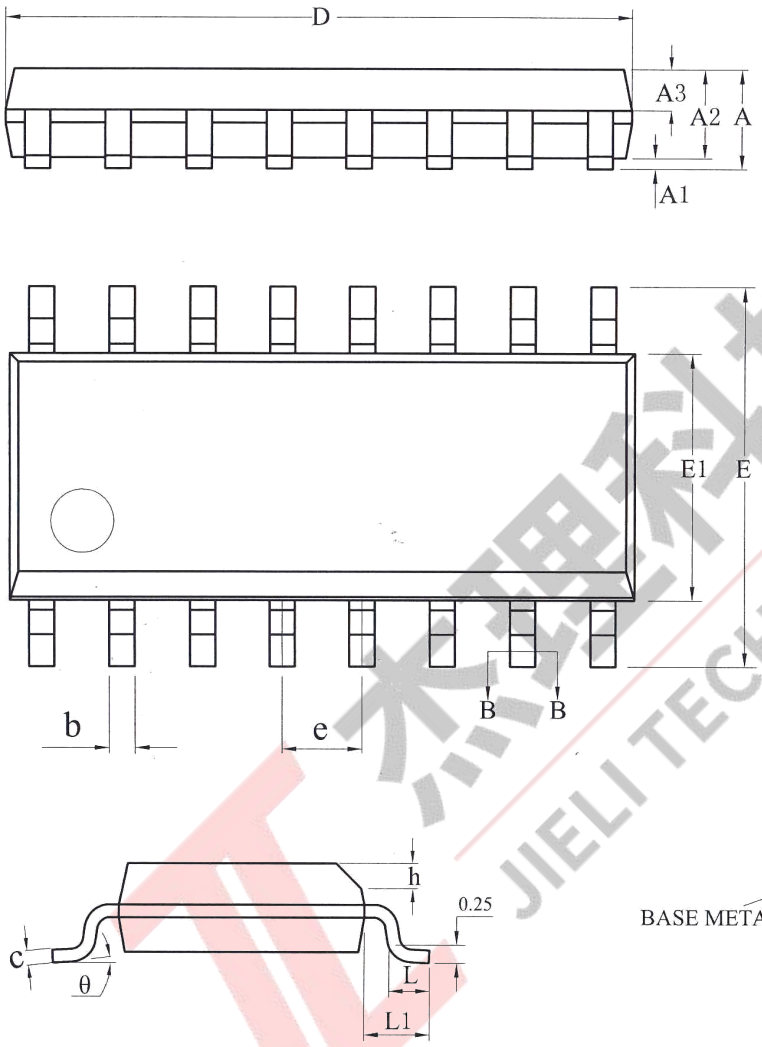
3.8 Internal Resistor Characteristics

Table 3-8

Port	**Internal Pull-Up Resistor**	**Internal Pull-Down Resistor**	**Comment**
P00~P03,P10~P12,P16~P17,P24	10K	10K	1. P00 default pull down 2. Internal pull-up/pull-down resistance | accuracy ±20%

4 Package Information

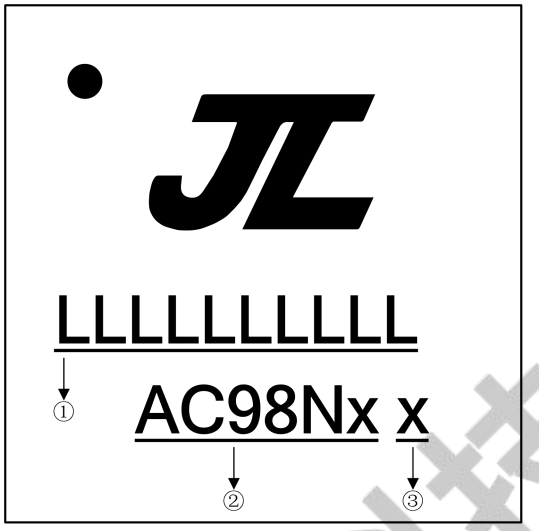
4.1 SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 4-1 AC983A Package

5 IC Marking Information



① LLLLLLLLLL：Production Batch
② AC98Nx：Chip Model
③ Built-in flash size
0: No Flash Memory
1: 1Mbit Flash

6 Solder-Reflow Condition

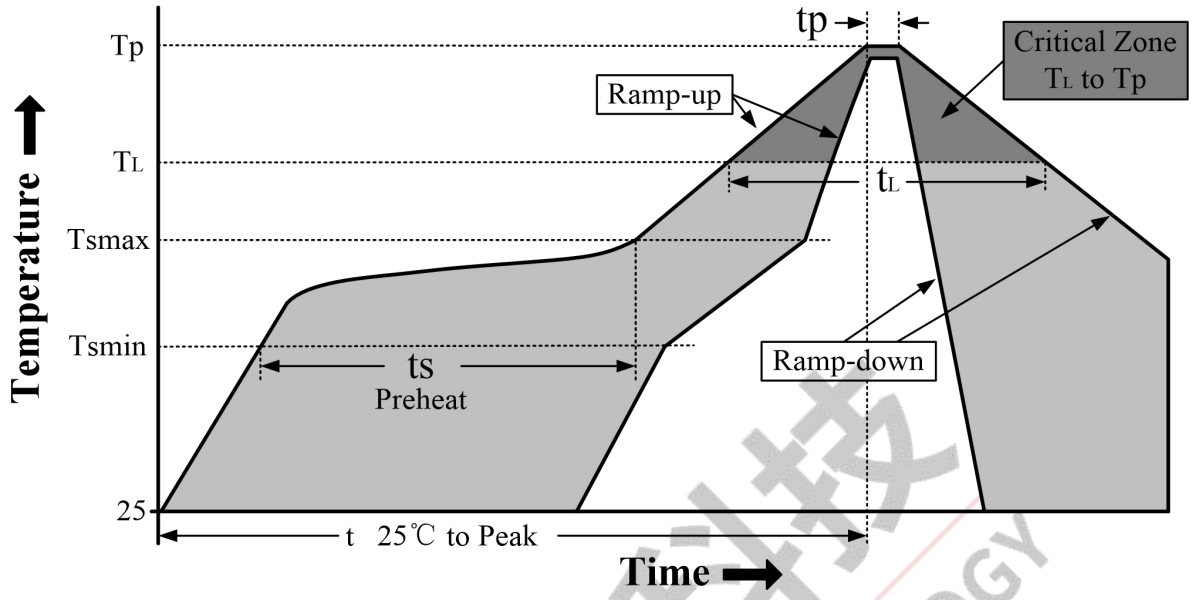


Figure 6-1 Classification Reflow Profile

Classification Profiles **Table 6-1**

Profile Feature		Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/ Soak	Temperature Min (T_{smin})	100 ℃	150 ℃
	Temperature Max (T_{smax})	150 ℃	200 ℃
	Time (ts) from (T_{smin} to T_{smax})	60-120 seconds	60-180 seconds
Average ramp-up rate (T_{smax} to T_p)		3 ℃/second max	3 ℃/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L		183 ℃ 60-150 seconds	217 ℃ 60-150 seconds
Peak package body temperature (T_p)		See Table 6-2.	See Table 6-3.
Time within 5°C of actual Peak Temperature (tp)		10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)		6 ℃/second max.	6 ℃/second max.
Time 25 ℃ to peak temperature		6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.

Note 2: Time within 5℃ of actual peak temperature (tp) specified for the reflow profiles is a “supplier” minimum and “user” maximum.

SnPb - Classification Temperature **Table 6-2**

Package Thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
<2.5 mm	240 +0/-5 ℃	225 +0/-5 ℃
≥ 2.5 mm	225 +0/-5 ℃	225 +0/-5 ℃

Pb-free - Classification Temperature **Table 6-3**

Package Thickness	Volume mm^3 < 350	Volume mm^3 350 - 2000	Volume mm^3 > 2000
< 1.6mm	260 ℃	260 ℃	260 ℃
1.6 mm - 2.5mm	260 ℃	250 ℃	245 ℃
> 2.5mm	250 ℃	245 ℃	245 ℃

7 Storage Condition

7.1 Moisture Sensitivity Level

AC983A is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-033.

7.2 Storage Alert

1. Calculated shelf life in sealed bag 12 months at＜40°C and 90% relative humidity (RH).
2. Peak package body temperature≤260°C.
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions≤30°C/60%RH or stored per J-STD-033.
4. Devices require bake before mounting if humidity indicator card reads ＞ 10% for level 2a-5a devices or＞60% for level 2 devices when read at 23±5°C,or 3a or 3b are not met.

Please refer to IPC/JEDEC J-STD-033 for baking procedure if necessary.

8 Revision History

Date	Revision	Description
2023.11.17	V1.0	Initial Release.