

AC6969T Datasheet

Zhuhai Jieli Technology Co.,LTD

Version: V1.1

Date: 2026.03.21

Copyright © Zhuhai Jieli Technology Co.,LTD. All rights reserved.

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

AC6969T Features

CPU

- 32-bit DSP supports hardware Float Point Unit(FPU)
- Up to 160MHz programmable processor
- 64Vectored interrupts
- 4 Levels interrupt priority

DSP Audio Processing

- SBC, AAC Audio decodes supported for BT audio
- mSBC voice codec supported for BT phone
- Supports MP2, MP3, WMA, APE, FLAC, AAC, MP4, M4A, WAV, AIF, AIFC audio decoding
- Packet Loss Concealment (PLC) for voice processing
- Acoustic echo cancellation/suppression (AEC,AES)
- Single analog Environmental Noise Cancellation (ENC)
- Multi-band DRC limiter
- 10-band EQ configuration for voice Effects

Audio Codec

- One channels 16-bit DAC, SNR >= 95dB
- One channels 16-bit ADC , SNR >= 90dB
- Sampling rates of 8KHz/11.025KHz/16KHz/22.05KHz/24KHz/32KHz/44.1KHz/48KHz are supported
- One analog MIC amplifier, build-in MIC bias Generator
- Supports two PDM digital MIC inputs
- Two channel analog MUX
- Supports cap-less, single-ended mode at the DAC path
- Supports 16ohm and 32ohm Speaker loading

Bluetooth

- Compliant with Bluetooth V6.0+BR+EDR+BLE specification (DN Q334307)

- Meet class2 and class3 transmitting power requirement
- Support GFSK and $\pi/4$ DQPSK all packet types
- Provides +6dbm transmitting power receiver with -90dBm sensitivity
- Fast AGC for enhanced dynamic range
- Supports a2dp\avctp\avdtp\avrcp\hfp\spp\smpl\att\gap\gatt\rfcomm\sdpl2cap profile a2dp 1.4\avctp 1.4\avdtp 1.3\ avrcp 1.6.3\ hfp 1.9\spp 1.2\rfcomm 1.2\pnp 1.3\ hid 1.1.1\sdpl2cap core 6.0\l2cap core 6.0

Peripherals

- One full speed USB 2.0 OTG controller
- Six multi-function 32-bit timers, support capture and PWM mode
- Three full-duplex basic UART, UART0 and UART1 supports DMA mode
- One SPI interface supports host and device mode
- One SD Card Host controller
- One hardware IIC interface supports host and device mode
- 10-bit ADC for analog sampling
- External wake up/interrupt on all GPIOs

PMU

- Low voltage LDO for internal digital and analog circuit supply
- 3uA current consumption in the soft-off mode
- Built-in LDO for the core, I/O, Bluetooth and flash
- VBAT is 2.2V to 4.5V
- IOVDD is 2.2V to 3.6V

Packages

- SOP16

Confidential

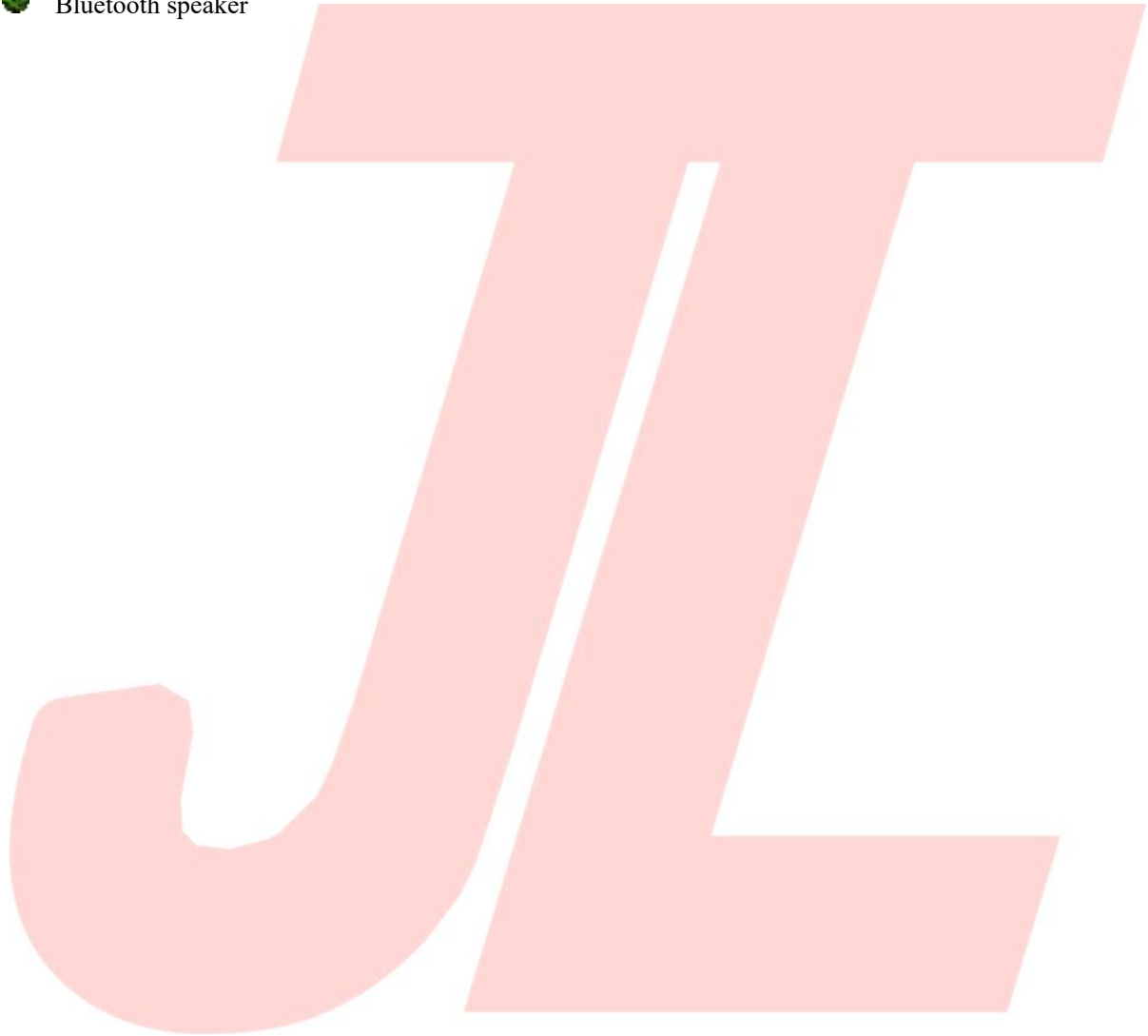
The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

Temperature

- Operating temperature: -40°C to +85°C
- Storage temperature: -65°C to +150°C

Applications

- Bluetooth speaker



1、 Pin Definition

1.1 Pin Assignment

DACR/PB7/PB6	○			16	VCOM
LDO_IN/PB5	1			15	VSS
VBAT	2			14	PA1
IOVDD	3			13	PA0/PA2
PB3/PB1	4	AC6969T		12	USBDP/PA4/PA5
BTRF	5	(SOP16)		11	USBDM/PC3
XOSCI	6			10	PC4
XOSCO	7			9	PC5
	8				

Figure 1-1 AC6969T_SOP16 Package Diagram

1.2 Pin Description

Table 1-1 AC6969T_SOP16 Pin Description

PIN NO.	Name	I/O Type	Drive (mA)	Function	Other Function
1	DACR	O	/		DAC Right Channel
	PB7	I/O	24/8	GPIO	AMUX1R: Analog Channel1Right; IIC_SDA_C: IIC DAT(C); ADC9: ADC Input Channel 9; PWM5: Timer5 PWM Output; UART1RXA: Uart1 Data In(A);
	PB6	I/O	24/8	GPIO	AMUX1L: Analog Channel1 Left; IIC_SCL_C: IIC SCL(C); ADC8: ADC Input Channel 8; TMR3: Timer3 Clock Input; UART1TXA: Uart1 Data Out(A);
2	LDO_IN	P	/		Battery Charger Power In
	PB5	I/O	/	GPIO (High Voltage Resistance)	PWM3: Timer3 PWM Output; CAP1: Timer1 Capture; UART0TXC: Uart0 Data Out(C); UART0RXC: Uart0 Data In(C);
3	VBAT	P	/		Power Supply
4	IOVDD	P	/		IO Power 3.3v
5	PB3	I/O	24/8	GPIO	PWM2: Timer2 PWM Output; ADC6: ADC Input Channel 6;
	PB1	I/O	24/8	GPIO (pull up)	Long Press Reset; ADC5: ADC Input Channel 5; TMR2: Timer2 Clock Input;
6	BT_RF	/	/		BT Antenna
7	BT_OSCI	I	/		BT OSC In
8	BT_OSCO	O	/		BT OSC Out
9	PC5	I/O	24/8	GPIO	SD0CLKA: SD0 Clock(A); SPI1DOB: SPI1 Data Out(B); IIC_SDA_B: IIC SDA(B); ADC12: ADC Input Channel 12; TMR1: Timer1 Clock Input; UART2RXD: Uart2 Data In(D);

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

10	PC4	I/O	24/8	GPIO	SD0CMDA: SD0 Command(A); SPI1CLKB: SPI1 Clock(B); IIC_SCL_B: IIC SCL(B); ADC11: ADC Input Channel 11; PWM1: Timer1 PWM Output; UART2TXD: Uart2 Data Out (D);
11	USBDM	I/O	4	USB Negative Data (pull down)	IIC_SDA_A: IIC SDA(A); ADC14: ADC Input Channel 14; UART1RXD: Uart1 Data In(D);
	PC3	I/O	24/8	GPIO	SD0DAT0A: SD0 Data0(A); SPI1DIB: SPI1 Data In(B); CAP2: Timer2 Capture; UART0TXD: Uart0 Data Out (D); UART0RXD: Uart0 Data In(D);
12	USBDP	I/O	4	USB Positive Data (pull down)	IIC_SCL_A: IIC SCL(A); ADC13: ADC Input Channel 13; UART1TXD: Uart1 Data Output(D);
	PA5	I/O	24/8	GPIO	PWM0: Timer0 PWM Output;
	PA4	I/O	24/8	GPIO	AMUX0R: Analog Channel0 Right; ADC3: ADC Input Channel 3; TMR4: Timer4 Clock Input;
13	PA2	I/O	24/8	GPIO	MIC_BIAS: Microphone Bias Output CAP3: Timer3 Capture;
	PA0	I/O	/	GPIO	SDPG: SD Power Supply ADC0: ADC Input Channel 0; CLKOUT0 UART1TXC: Uart1 Data Output(C);
14	PA1	I/O	24/8	GPIO	MIC: MIC Input Channel ; ADC1: ADC Input Channel 1; PWM4: Timer4 PWM Output; UART1RXC: Uart1 Data In(C);
15	VSS	P	/		Ground
16	VCOM	/	/		DAC Reference Output

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2、Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1

Symbol	Parameter	Min	Max	Unit
Tamb	Operating Temperature	-40	+85	°C
Tstg	Storage temperature	-65	+150	°C
VBAT	Supply Voltage	-0.3	4.5	V
LDO_IN	Charger Voltage	-0.3	5.5	V
V _{3.3IO}	3.3V IO Input Voltage	-0.3	IOVDD+0.3	V

Note : The chip can be damaged by any stress in excess of the absolute maximum ratings listed below

2.2 PMU Characteristics

Table 2-2

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
VBAT	Voltage Input	2.2	3.7	4.5	V	VBAT = 4.2V
LDO_IN	Charger Voltage	-	-	300	mA	
V _{3.3IO}	Voltage output		3.3		V	VBAT = 4.2V, 100mA loading

2.3 Battery Charge

Table 2-3

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LDO_IN	Voltage Input	4.5	5	5.5	V	-
V _{Charge}	Charger Voltage	4.15	4.2	4.25	V	-
I _{Charge}	Charge Current	20		300	mA	Charge current at fast charge mode
I _{Trinkl}	Trickle Charge Current	20	45	70	mA	VBAT < V _{Trinkl}

2.4 IO Input/Output Electrical Logical Characteristics

Table 2-4

IO input characteristics						
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V _{IL}	Low-Level Input Voltage	-0.3	–	0.3* IOVDD	V	IOVDD = 3.3V
V _{IH}	High-Level Input Voltage	0.7* IOVDD	–	IOVDD+0.3	V	IOVDD = 3.3V
IO output characteristics						
V _{OL}	Low-Level Output Voltage	–	–	0.33	V	IOVDD = 3.3V
V _{OH}	High-Level Output Voltage	2.7	–	–	V	IOVDD = 3.3V

2.5 Internal Resistor Characteristics

Table 2-5

Port	General Output	High Drive	Internal Pull-Up Resistor	Internal Pull-Down Resistor	Comment
PA1, PA4, PA5 PB1, PB3, PB5~PB7 PC3~PC5	8mA	24mA	10K	10K	1、PB1 default pull up 2、USBDM & USBDP default pull down 3、PB5 can pull-up resistance to 5V 4、internal pull-up/pull-down resistance accuracy ±20%
PB3 PA0	Output0 8mA	24mA	10K	10K	
	Output1 8mA	64mA			
PB5	8mA	–	10K	10K	
USB DP	4mA	–	1.5K	15K	
USB DM	4mA	–	180K	15K	

2.6 DAC Characteristics

Table 2-6

Parameter	Min	Typ	Max	Unit	Test Conditions
Frequency Response	20	–	20K	Hz	1KHz/0dB 10Kohm loading With A-Weighted Filter
THD+N	–	-75	–	dB	
S/N	–	95	–	dB	
Output Swing		1		V _{rms}	
Dynamic Range		95		dB	1KHz/-60dB 10Kohm loading With A-Weighted Filter
DAC Output Power		20	–	mW	32ohm loading

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

2.7 ADC Characteristics

Table 2-7

Parameter	Min	Typ	Max	Unit	Test Conditions
Dynamic Range		80		dB	Fsample=44.1kHz Fin=1KHz 2mVpp Input
S/N	–	90	91	dB	Fsample=44.1kHz
THD+N	–	-70	–	dB	Fin=1KHz 1.2Vpp Input

2.8 BT Characteristics

2.8.1 Transmitter

Basic Data Rate

Table 2-8

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Transmit Power		4	6	dBm	25°C, Power Supply VBAT=3.7V 2441MHz
RF Power Control Range		20		dB	
20dB Bandwidth		950		KHz	
Adjacent Channel	+2MHz	-40		dBm	
	-2MHz	-38		dBm	
Transmit Power	+3MHz	-44		dBm	
	-3MHz	-35		dBm	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

Enhanced Data Rate**Table 2-9**

Parameter		Min	Typ	Max	Unit	Test Conditions
Relative Power			-1		dB	25°C, Power Supply VBAT=3.7V 2441MHz
$\pi/4$ DQPSK Modulation Accuracy	DEVM RMS		6		%	
	DEVM 99%		10		%	
	DEVM Peak		15		%	
Adjacent Channel	+2MHz		-40		dBm	
	-2MHz		-38		dBm	
Transmit Power	+3MHz		-44		dBm	
	-3MHz		-35		dBm	

2.8.2 Receiver**Basic Data Rate****Table 2-10**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=3.7V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
Interference Rejection	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Enhanced Data Rate**Table 2-11**

Parameter		Min	Typ	Max	Unit	Test Conditions
Sensitivity			-90		dBm	25°C, Power Supply VBAT=3.7V 2441MHz
Co-channel Interference Rejection			-13		dB	
Adjacent Channel	+1MHz		+5		dB	
	-1MHz		+2		dB	
	+2MHz		+37		dB	
Interference Rejection	-2MHz		+36		dB	
	+3MHz		+40		dB	
	-3MHz		+35		dB	

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.

3、 Package Information

3.1 SOP16

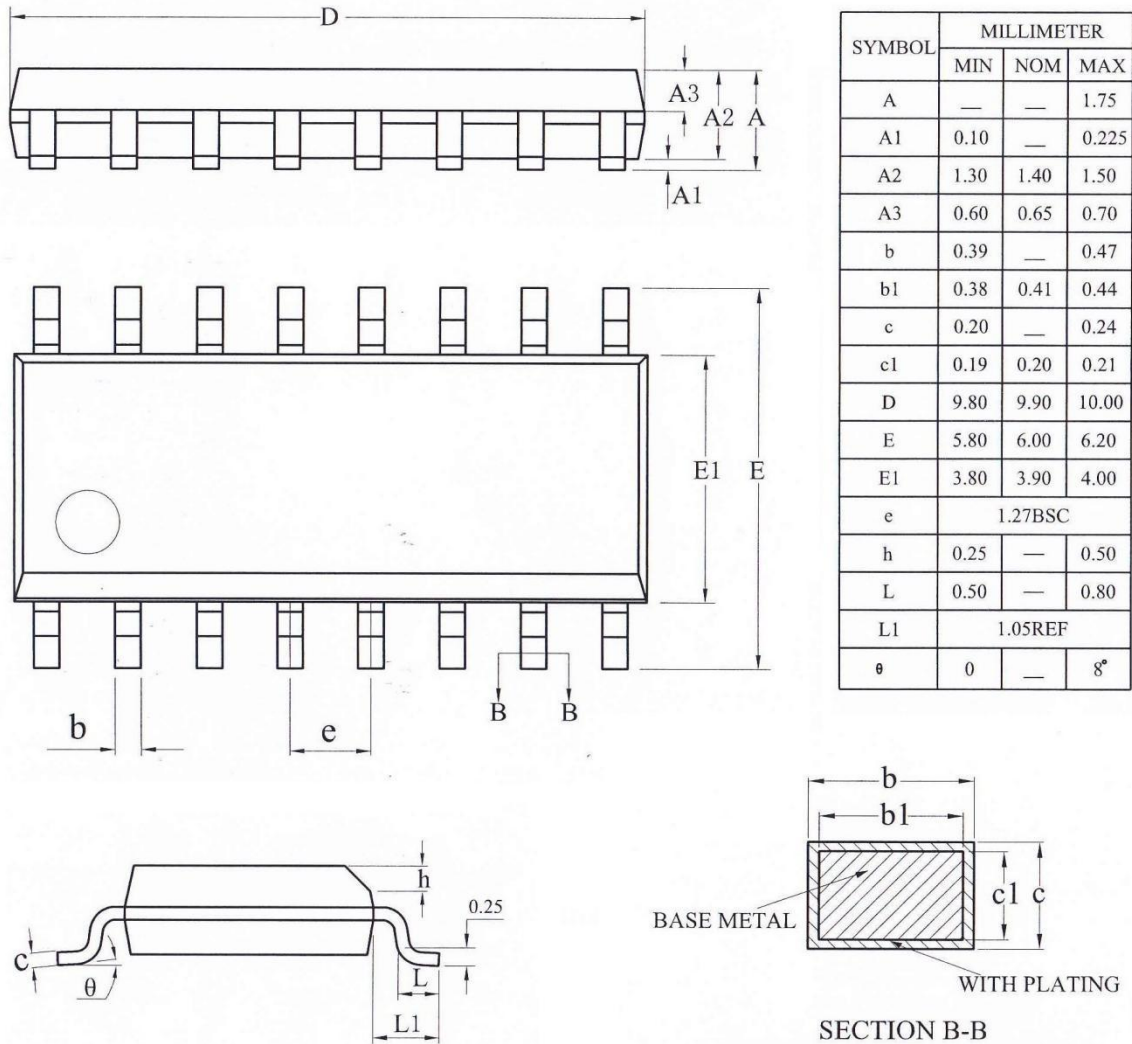


Figure 3-1. AC6969T_SOP16 Package

4、 Revision History

Date	Revision	Description
2025.12.15	V1.0	Initial Release
2026.03.21	V1.1	Update PMU Characteristics

Confidential

The information contained herein is the exclusive property of JIELI and shall not be distributed, reproduced, or disclosed in whole or in part without prior written permission of JIELI.